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Date: 9/17/2020

# Submission Instructions:

## Prelab:

1. Complete the prelab (questions Q1 and Q2)
2. Submit this report with the prelab completed to Canvas **before** your lab starts

## Lab:

1. Complete the lab according to the instructions
2. Take screenshots of your ModelSim waveform (note: to receive points your NetID has to be present in the screenshot) and insert them into this document.

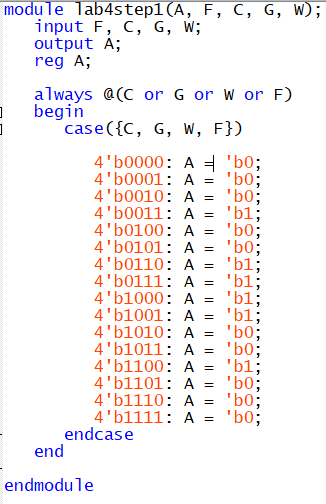
Complete this report and reupload it to Canvas.

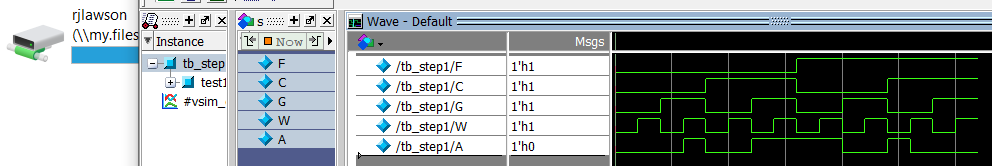
**PRELAB:**

**Q1.** Consider the Verilog code in section 3.0. Briefly explain how the **always @** structure works.

Always: blocks are used to describe events that should happen certain condition.

**Q2**. Write the Verilog code for ***lab4step1***. Use the example code given in Section 3.0 and make the necessary changes.





**Q3**. Read Section 4.0 and fill in the Truth Table for ***lab4step2***.

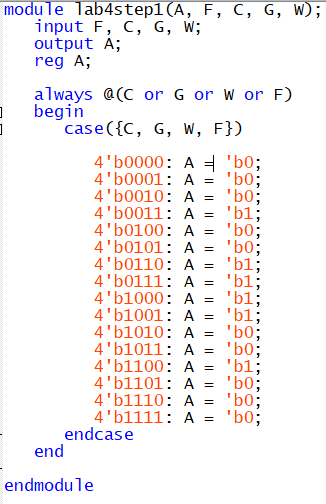
|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Inputs** | | | | **Outputs** | | |
| **M** | **T** | **H** | **P** | **E** | **F** | **AC** |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 |

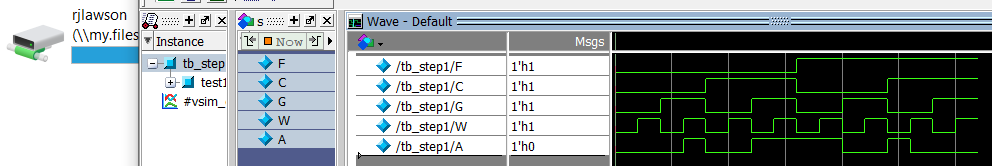
**LAB:  
3.0** Use the hardware results to fill in the truth table for ***lab4step1.***

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Farmer** | **Cabbage** | **Goat** | **Wolf** | **Alarm** |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 |

Screenshots:

**<<<Copy and paste your Verilog code here>>>**





**4.0**  Demonstrate hardware results for correct code.

**<<<Insert a screen shot of your lab4step2 BDF file>>>**

Design result:

